REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claim 1 has been amended and claims 49 and 50 have been added. All the amendments and new claims are supported by the original specification, for example at paragraphs 0011-0018 and Figures 2A-2C. No new matter is being added. Thus, upon entry of this reply, claims 1-50 will remain pending in the application.

Claims rejections - 35 U.S.C. § 102 and § 103

Claims 1-6, 11,-13, 15-16, 32, and 40-46 were rejected as being allegedly anticipated under 35 U.S.C. § 102 BY U.S. Patent No. 6,470,437 to Lyon ("Lyon patent" or "Lyon"). Claims 7-10, 14, 17-31, 33-39, and 47 were rejected as being allegedly obvious under 35 U.S.C. § 103 in light of Lyon.

This application discloses techniques for extending the local memory address space of a processor. In an embodiment, a processor may include a local addressable memory, such as an SRAM, in parallel with L1 local cache. A local memory controller may examine a local memory descriptor to determine whether a page containing a requested memory location is in the local addressable memory. If the requested memory location is not in the local addressable memory, the local memory controller may route the access to the local cache instead.

In contrast, Lyon describes the internal design of a cache itself. Indeed, the figures in Lyon are diagrams of different cache architecture designs. Lyon does not disclose the design of a memory structure external to a cache.

The bulk of the Office Action relies on equating a cache or elements within a cache of Lyon with the local addressable

memory recited in the pending claims. However, the application makes clear several distinctions between a local addressable memory and a cache. Therefore, the recited local addressable memory is very different from the cache in Lyon.

For example, paragraph 0012 of the present application states: "The processor core 105 may include local (L1) addressable memory, e.g., an L1 SRAM . . . . Unlike the L1 caches, the L1 SRAMs are 'real' memory and will return requested information if it exists. Thus, accesses to L1 SRAM may not entail cache misses and the associated penalties."

Paragraph 0018 of the present application also provides supports that local addressable memory is an entirely different entity from cache. For example, "local memory exists in parallel with local cache, making it unnecessary to send the access to both the L1 cache and L1 SRAM simultaneously." A structure can only exist in parallel with a different structure; it cannot exist in parallel with itself.

Similarly, in the same paragraph: "local memory requests are routed immediately to the L1 SRAM[,] and the L1 cache does not receive such requests." The fact that a request that reaches the local addressable memory (L1 SRAM) is not received by the cache (L1 cache) further makes clear the local addressable memory and the cache must be different structures. The written description thus makes abundantly clear that the local addressable memory is not a cache and is different from a cache in structure and in operation.

Applicants may act as their own lexicographers. See M.P.E.P. § 2173.01. In this case, Applicants have made clear that a local addressable memory is different from a cache. Moreover, even if Examiner disagrees that the definition is explicit, even an implicit definition is sufficient. "The specification should also be relied on for more than just

explicit lexicography or clear disavowal of claim scope to determine the meaning of a claim term when applicant acts as his or her own lexicographer; the meaning of a particular claim term may be defined by implication, that is, according to the usage of the term in context in the specification. See Phillips v. AWH Corp., __F.3d__, 75 USPQ2d 1321 (Fed. Cir. 2005) (en banc); and Vitronics Corp. v. Conceptronic Inc., 90 F.3d 1576, 1583, 39 USPQ2d 1573, 1577 (Fed. Cir. 1996)." M.P.E.P. § 2111.01.

All of the claim rejections in the Office Action were based on equating local addressable memory and cache. However, because Applicants' definition of local addressable memory excludes a cache, all claims are believed to be distinctly different from the cited prior art and thus are in a condition for allowance.

Nevertheless, Applicants have amended claim 1 and added new claims 49-50 to make even more clear that local addressable memory is different from the cache or structures within a cache of Lyon. Accordingly, the claimed subject matter is distinctly different from, and neither anticipated nor made obvious by, the cache designs discussed by Lyon.

Conclusion

Applicants respectfully submit that all rejections have been fully addressed and obviated. Accordingly, the application is now in a full condition for allowance. A Request for Continued Examination (RCE) is filed herewith in order for the new amendments to be considered.

Attorney's Docket No.:10559-566001

Please apply a fee of $790 for request for continued examination, a fee of $50 for excess claim fee and a fee of $450 for an extension of time for 2 months, and any other applicable charges or credits, to Deposit Account No. 06-1050.

Respectfully submitted,

Date: December 15, 2005

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